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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,716	10/21/2003	Li-Chun Tu	MTKP0050USA	2715

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EXAMINER	
MCFADDEN, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,716	TU ET AL.	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/7/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-13 are pending in the Application.

Request for Continued Examination

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 May 2006 has been entered.

Response to Amendment

3. Applicant's arguments filed on 11 May 2006 have been fully considered but they are not persuasive.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 7 March 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) further in view of Barlow et al (herein Barlow (U.S. Patent No. 6,311,263)).

7. **Regarding Claim 1**, Welfeld discloses a processor comprising:

A data memory storing for non-stack data (Figure 5, element 110 see column 8, lines 43-46);

A stack memory for storing stack data, where the stack memory is different from the data memory, (Figure 5, element 120 labeled Stack Memory, see column 9, lines 16-19);

A memory address generator coupled to the data memory for producing addresses to access the data memory; and

A stack pointer generator coupled to the stack memory for producing stack pointers to access the stack memory; and

A central processing unit (CPU) coupled to the memory address generator and the stack pointer generator, the central processing unit for processing

non-stack data and stack data according to an instruction set. (Figure 5, element 130);

8. Welfeld fails to disclose wherein the stack pointer generator is further for producing a software stack pointer to access the stack memory when passing parameters to subroutines of the central processing unit.

9. Barlow discloses wherein the stack pointer generator is further for producing a software stack pointer to access the stack memory when passing parameters to subroutines of the central processing unit. (See Column 15, Line 65 – Column 16, Line 5).

10. The memory address generator and the stack pointer generator are inherently disclosed in Welfeld. Meaning that although the claimed elements are not expressly disclosed in the reference, they must be a part of the reference. In order to access memory addresses in the data memory there must be a memory address generator to provide the addresses used. Also, to be able to add and delete elements from the stack memory there must be a stack pointer generator to access the stack memory.

11. Welfeld and Barlow are analogous art because they are from the same field of endeavor, microprocessors.

12. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the software controlled stack pointer capability of Barlow in the system of Welfeld.

13. The motivation for doing so would have been to make the memory cycles of the stack memory of Welfeld more efficient. The stack requires data stored in the programmable memory relating to the next state and therefore executes a stack access and programmable memory access to switch states. **(Column 3, Lines 21-28)**

14. Therefore it would have been obvious to combine the software controlled stack pointer capability of Barlow in the system of Welfeld for the benefit of more efficient memory cycles to obtain the invention as specified in Claim 1.

15. **Claim 7 is rejected using the same rationale as Claim 1.**

16. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) further in view of Barlow et al (herein Barlow (U.S. Patent No. 6,311,263)) and Microsoft Computer Dictionary (used as an evidentiary reference):

17. **Regarding Claim 2**, Welfeld discloses the processor of claim 1 wherein the processor is a microcontroller (figure 5, element 100 see column 8, lines 30-32);

Although not expressly disclosed as such the Examiner respectfully asserts that the integrated circuit of Welfeld is a microcontroller.

A microcontroller is defined as a microprocessor on a single integrated circuit, which may also include small amounts of memory, timers, and I/O ports (Microsoft Computer Dictionary, page 337).

It can then be seen that the integrated circuit of Welfeld includes a processor along with a programmable memory, a stack memory, a

RAM arbiter, and a memory programmer all on a single integrated circuit, therefore, making it a microcontroller.

18. **Claim 8 is rejected using the same rationale as Claim 2.**

19. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) and Barlow et al. (U.S. Patent No. 6,311,263) as applied to claim 1 above, and further in view of Anderson et al. (hereinafter Anderson (U.S. Patent No. 3,969,724)).

Regarding Claim 3, Welfeld and Barlow et al. fail to disclose the processor of claim 1 wherein the processor processes an 8-bit instruction set;

Anderson discloses the processor of claim 1 wherein the processor processes an 8-bit instruction set (Figure 1, element 10 and column 23, lines 1-2);

Welfeld, Barlow, and Anderson are analogous art because they are from the same field of endeavor, microprocessors;

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the processor of Welfeld (Figure 5, element 130) with the central processing unit of Anderson (Figure 1, element 10;

The motivation for doing so would have been to perform data processing operations faster than before;

Therefore it would have been obvious to combine the central processing unit of Anderson with the integrated circuit of Welfeld and Barlow in place of the processor (Figure 5, element 130) of Welfeld to perform data processing operations faster than before;

20. **Claim 9 is rejected using the same rationale as Claim 3.**

21. Claims 4, 5, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047), Barlow et al. (U.S. Patent No. 6,311,263), and Anderson (U.S. Patent No. 3,969,724) as applied to claim 3 above, and further in view of Shima et al. (hereinafter Shima (U.S. Patent No. 4,332,008)).

Regarding Claim 4, Welfeld, Barlow, and Anderson fail to disclose the processor of claim 3 wherein the data memory is 256 bytes.;

Shima discloses the data memory that is 256 bytes (column 6, lines 15-18);

Welfeld, Barlow, Anderson, and Shima are from analogous art because they are from the same field of endeavor, microprocessors;

At the time of invention it would have been obvious to a person of ordinary skill in the art to replace the programmable memory from Welfeld (Figure 5, element 110) with the data memory from Shima.

The motivation for doing so would have been that most computer systems require some amount of external Read/Write memory for data storage and to implement a “stack” (column 6, lines 15-17);

Therefore it would have been obvious to combine the data memory of Shima with the integrated circuit of Welfeld, Barlow, and Anderson to provide the external Read/Write memory, for data storage and implementing a "stack", that most computers require.

Regarding Claim 5, Welfeld, Barlow, and Anderson fail to disclose the processor of claim 3 wherein the stack memory is 256 bytes.;

Shima discloses the stack memory that is 256 bytes (column 6, lines 15-18);

Welfeld, Barlow, Anderson, and Shima are from analogous art because they are from the same field of endeavor, microprocessors;

At the time of invention it would have been obvious to a person of ordinary skill in the art to replace the stack memory from Welfeld (Figure 5, element 110) the stack memory from Shima.

The motivation for doing so would have been that most computer systems require some amount of external Read/Write memory for data storage and to implement a "stack" (column 6, lines 15-17);

Therefore it would have been obvious to combine the data memory of Shima with the integrated circuit of Welfeld, Barlow, and Anderson to provide the external Read/Write memory, for data storage and implementing a "stack", that most computers require.

Shima is used for both claim 4 and claim 5 because the reference discloses both uses for the memory, data and stack, at the size specified.

When the programmable memory and stack memory of Welfeld are replaced with the external Read/Write memory of Shima then both memories are 256 bytes as specified in claims 4 and 5.

22. **Claim 10 is rejected using the same rationale as Claim 4.**

23. **Claim 11 is rejected using the same rationale as Claim 5.**

24. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welfeld (U.S. Patent No. 6,167,047) and Barlow et al. (U.S. Patent No. 6,311,263) as applied to claims 1 and 7 above, and further in view of Applicant admitted prior art (herein AAPA).

25. **Regarding Claim 6,** Welfeld and Barlow fail to disclose wherein the stack pointer generator is further for incrementally increasing the stack pointer to point to a next address when used by the central processing unit, and for decreasing the software stack pointer from a predetermined starting position when passing parameters to subroutines of the central processing unit.

26. AAPA discloses wherein the stack pointer generator is further for incrementally increasing the stack pointer to point to a next address when used by the central processing unit, and for decreasing the software stack pointer from a predetermined starting position when passing parameters to subroutines of the central processing unit. **(See AAPA Section 6 and Figure 2.)**

27. Welfeld, Barlow, and AAPA are analogous art because they are from the same field of endeavor, microprocessors.

28. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the capability of the stack pointer and software stack pointer functioning simultaneously within the stack memory of AAPA with the stack memory of Welfeld and Barlow.

29. The motivation for doing so would have been when calling subroutines, many programs need to send parameters and use a software stack pointer to store those parameters. **(AAPA: Section 6, Lines 15-18)**

30. Therefore it would have been obvious to combine the simultaneous stack and software stack function with the stack memory of Welfeld and Barlow to provide the necessary memory that many subroutines and programs need to send and store parameters.

31. **Claim 12 is rejected using the same rationale as Claim 6.**

32. **Claim 13 is a combination of Claims 1, 4, and 5 and is therefore rejected upon the same rationale.**

Response to Arguments

33. Applicant's arguments filed 11 May 2006 have been fully considered but they are not persuasive.

34. Applicant argues that "the Y register of Barlow must be included into the processor of Welfeld" and therefore "the processor 130 of Welfeld must be entirely replaced with the processor core 100 of Barlow." However the Office states that only the

capability of the register is incorporated into the system of Welfeld. **(Paragraph 12 of the present Action)** The register itself is not incorporated into the system of Welfeld. The system of Welfeld is therefore kept intact and the capability and functionality of a software stack pointer is added.

35. The remainder of the Applicant's arguments depend on the replacement of the processor core of Welfeld. The processor core of Welfeld is not replaced. Therefore the Applicant's arguments are moot.

36. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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6/7/06

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5/31/2006

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SUPERVISORY PATENT EXAMINER